EE 435

Homework 5

Spring 2025 (Due Wednesday Mar 5)

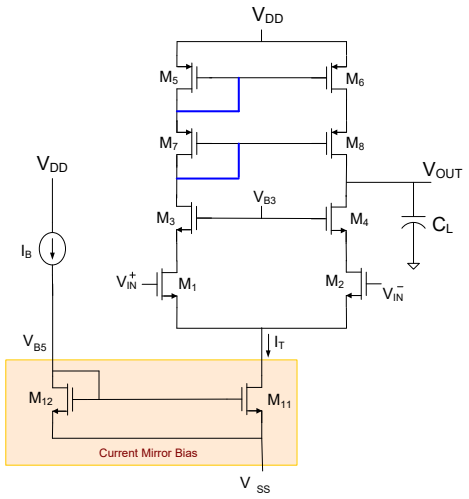
In the following problems, if reference to a semiconductor MOS process is needed, assume a processes with characteristics: CMOS Process -- $\mu_n C_{OX}=250\mu A/v^2$, $\mu_p C_{OX}=\mu_n C_{OX}$ /3 , $V_{TNO}=0.4V$, $V_{TPO}= - 0.4V$, $C_{OX}=2fF/\mu^2$, $\lambda_n= \lambda p= 0.01V^{-1}$, $\gamma = 0.4V^{-1/2}$, and $\max(V_{DD}-V_{SS})=3.6V$. For a bipolar Process assume $J_S=10^{-15}A/\mu^2$, $\beta=100$ and $V_{AF}=150V$.

Problem 1 4.14 Martin and Johns

Problem 2 5.2 Martin and Johns

Problem 3 Consider problem 5.5 of Martin and Johns but replace the "will they be stable or unstable when used with negative feedback ...." with
Where will the closed-loop poles and zeros be if used in a basic noninverting voltage feedback amplifier with a nominal gain with feedback of 2.
Where will the closed-loop poles and zeros be if used in a basic inverting voltage feedback amplifier with a nominal gain with feedback of -2?

Problem 4 Determine the slew rate of the telescopic cascode amplifier shown below if $V_{DD}=1.8V$, $V_{SS}=-1.8V$, $I_B=1mA$ and the excess bias on all transistors in 300mV.



Problem 5 Assume the amplifier in Problem 4 is designed so that the excess bias of all transistors is 300mV , $V_{DD}=1.8V$, $V_{SS}= -1.8V$, and the power dissipation is 25uW,

a) Determine the ac voltage gain
b) Determine all of the natural design parameters for this amplifier
c) Determine the GB if $C_L=2pF$
d) Determine the SR if $C_L=2pF$

Problem 6 Consider an amplifier with two inputs V_{IN1} and V_{IN2}. If V_{IN1}=.01sin1000t and V_{IN2}= -0.0101sin1000t, the output was 5sin1000t. When the inputs were V_{IN1}=0.01sin1000t and V_{IN2}= -.0102sin1000t the output was 4sin1000t.
Determine

a) The common-mode and difference-mode inputs for the first set of inputs
b) Determine the common-mode gain, A_C, and the difference mode gain, A_D
c) Determine the CMRR (CMRR=A_D/A_C)

Problem 7 Give the circuit schematic for a two-stage operational amplifier with a folded-cascode differential-input first stage with p-channel inputs and tail current bias and a cascode second stage with single-ended n-channel input and tail voltage bias.

Problem 8 Determine the gain for the amplifier in Problem 7 in terms of the small-signal model parameters of the devices.

Problem 9,10 Consider the 7T op amp shown below with V_{DD}=3.6V and the total power dissipation is 5mW with 90% of the total power dissipated in the last stage. Assume that V_{EB} on all transistors is 200mV and the load capacitor is C_L=1pF.

a) What is the dc voltage gain
b) Determine C_C so that the closed loop pole Q is 0.5 with a β=1.
c) What is the size of M_1?
d) What is the biasing voltage V_{B1}?
e) Determine the phase margin with the compensation capacitor C_C used in part b)
f) Determine the GB of the op amp with the compensation capacitor C_C determined in part b)
g) What are the open-loop poles?
h) Determine the closed loop poles for β=1 and the compensation capacitor CC used in part b)
i) What is the common-mode input range?
j) What is the output swing?